OUTPUT BUFFER ESD PROTECTION USING PARASITIC SCR PROTECTION CIRCUIT FOR CMOS VLSI INTEGRATED CIRCUITS

ABSTRACT

[0033] An input and output (I/O) circuit with an improved ESD protection is disclosed. The circuit has an output buffer having an NMOS transistor coupled to a PMOS transistor, an ESD protection circuit having a parasitic silicon controlled rectifier (SCR) integrated therein and coupled to the output buffer, and a diode string having a predetermined number of diodes coupled between a source node of the NMOS transistor and ground, wherein a voltage drop across the diode string increases the SCR gate holding voltage, thereby setting an ESD protection holding voltage for the ESD protection circuit.